depositing an insulator layer of high temperature oxide directly on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls around the floating gate to prevent charge leaking from the floating gate;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

3. The method of claim 1, wherein the thickness of the floating gate is between approximately 500Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

4. The method of claim 1, wherein polishing the insulator layer includes chemical mechanical polishing.

5. The method of claim 1, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

6. The method of claim 5, wherein depositing the dielectric layer includes depositing an ONO layer.

7. A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

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depositing a floating gate layer on the tunnel oxide to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

C1 Cont

9. The method of claim 7, wherein the first thickness is between approximately 500 Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

10. The method of claim 7, wherein polishing the insulator layer includes chemical mechanical polishing.

11. The method of claim 7, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

12. The method of claim 11, wherein depositing the dielectric layer includes depositing an ONO layer.

14. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped polysilicon.

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C1 Cncld

15. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped amorphous silicon.

21. The method of claim 1 wherein the layer of high temperature oxide is formed by LPCVD process.

C2

22. The method of claim 7 wherein the layer of high temperature oxide is formed by LPCVD process.

23. A method of making a flash memory cell including a substrate and a floating gate, the method comprising:

depositing an insulator layer of high quality oxide on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls of high quality oxide around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

REMARKS

Claims 1, 3-7, 9-12, 14 and 15 are pending in the application. Claims 1 and 7 are amended. New claims 21-23 are added. Support for the new claims can be found on page 4

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of the application. No new matter has been introduced. Claims 1, 3-7, 9-12, 14,15, 21-23 are pending for the Examiner's consideration.

Rejection of Claims Under 35 U.S.C. §102(b)

The Examiner rejected Claims 1, 5, 7 and 11 under 35 U.S.C. §102(b) as being anticipated by Mitchell *et al.*, U.S. Patent No. 4,713,142. The Examiner stated:

> "Mitchell *et al.* Discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6."

Applicants have amended Claim 1 to recite "depositing an insulator layer of high temperature oxide directly on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls around the floating gate to prevent charge leaking from the floating gate." Applicants' original claims and the Specification, page 4, lines 25-27 and FIGS. 5-7 support the added language. No new matter has been introduced.

no new matter

Mitchell *et al.* do not teach "depositing an insulator layer of high temperature oxide ***directly*** on the substrate and the floating gate . . . to prevent charge leaking from the floating gate" (emphasis added). To the contrary, insulator layer 37 disclosed in the cited reference is formed over an oxide layer 36, wherein oxide layer 36 is the layer that enhances "charge retention of the floating gate" (col. 2, ln. 68 and col. 3, lns. 1-3). Claim 1 is thus distinguishable over the cited reference because Claim 1's single "insulator layer of high temperature oxide" accomplishes the same effect as the two separate layers 36 and 37 taught by Mitchell *et al.*

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Further, Claim 1 further distinguish over Mitchell *et al.* by reciting other limitations not disclosed or suggested by Mitchell *et al.* For example, according to Mitchell *et al.*, neither the oxide layer 36 nor the insulator layer 37 is deposited to "a thickness greater than a thickness of the floating gate," as recited in Claim 1. As illustrated in FIGS. 2c and 2d of the cited reference, oxide layer 36 is a very thin layer formed over the floating gate and the thickness of insulator layer 37, at best, is substantially the same as the thickness of the floating gate.

not true

As another example, Mitchell *et al.* teach two separate steps to form an oxide layer 36 and an insulator layer 37 over a floating gate. Layer 37 acts to insulate and layer 36 acts to enhance a "charge retention of the floating gate" (col. 3, lns. 1-3). But, the method in accordance with Claim 1, advantageously, involves only one step to form a high temperature oxide serving to both insulate and prevent charges from leaking.

Thus, for the above reasons, Applicants request reconsideration and allowance of Claims 1 and 5.

During the telephonic interview of October 3, 2001, the Examiner indicated that Claim 1 of Mitchell *et al.* (column 4, lines 53-55) teaches "depositing a conformal layer of insulating material on the surface of said substrate and said conductive strips." Applicants submit that the Examiner is taking that teaching out of context. Taken as a whole, the cited reference teaches away from the present invention. For example, at column 4, lines 60-62, Mitchell *et al.* disclose "forming a layer of ***conductive material*** on the surface of said conformal layer" (emphasis added). In contrast, Claim 1 of the present invention recites "depositing a ***dielectric*** layer on the planar surface" (emphasis added). Since a dielectric layer is NOT conductive, the cited reference, when read in its entirety, teaches away and is patentably distinguishable from Claim 1 of the present invention.

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Claim 7 has been similarly amended, and recites "depositing an insulator layer of high temperature oxide directly on the substrate and the floating gate such that the insulator layer

has a thickness that is greater than the first thickness." Therefore, for substantially the reasons given above with respect to Claim 1, Claim 7 and dependent Claim 11 as amended are each allowable over the cited prior art.

Rejection of Claims Under 35 U.S.C. §103

The Examiner rejected Claims 1, 3-7, 9-12, 14-15 under 35 U.S.C. §103(a) as being unpatentable over Wu, U.S./6,033,956 or Yamagishi *et al.*, U.S./5,808,339 or Chan *et al.*, U.S./6,051,467 taken with Sze *et al.*, "ULSI Technology" and in view of Applicant's admitted prior art.

Applicants respectfully traverse the Examiner's rejection. MPEP §2143 provides:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.[1] In particular, because none of the cited references suggests or discloses a "high temperature oxide" or an LPCVD process for forming a single oxide layer over a floating gate that can act to both insulate the floating gate and prevent charges from leaking, the Examiner combination of Sze *et al.* and the cited references can only be made by hindsight. Obviousness may not be established by hindsight reconstruction or conjecture.[2]

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[1] In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

[2] ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984).

If the Examiner disagrees, Applicants respectfully request that the Examiner point out the suggestion or motivation to combine the cited references with more specificity in support of his section 103 rejection, as required under MPEP §2143.01 and §2143.03. A prima facie case of obviousness not being established, it is respectfully requested that section 103 rejection to be withdrawn.

Newly presented Claims 21-23 are believed each allowable over the cited prior art references of record.

For the reasons set forth above, all pending claims (i.e., Claims 1, 3-7, 9-12, 14-15 and 22-23) are believed allowable and, accordingly, their allowance is requested. If the Examiner has any question regarding the above, the Examiner is requested to telephone the undersigned at 408-453-9200.

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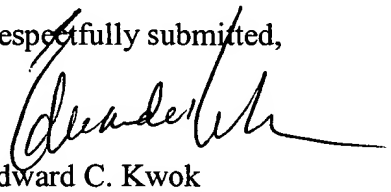

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ATTACHMENT A

1. **(TRICE AMENDED)** A method of making a flash memory cell including a substrate and a floating gate, the method comprising:

depositing an insulator layer of high temperature oxide directly on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls around the floating gate [operable] to prevent charge leaking from the floating gate;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

3. The method of claim 1, wherein the thickness of the floating gate is between approximately 500Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

4. The method of claim 1, wherein polishing the insulator layer includes chemical mechanical polishing.

5. The method of claim 1, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

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6. The method of claim 5, wherein depositing the dielectric layer includes depositing an ONO layer.

7. **(TRICE AMENDED)** A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

9. The method of claim 7, wherein the first thickness is between approximately 500 Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

10. The method of claim 7, wherein polishing the insulator layer includes chemical mechanical polishing.

11. The method of claim 7, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

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12. The method of claim 11, wherein depositing the dielectric layer includes depositing an ONO layer.

14. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped polysilicon.

15. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped amorphous silicon.

21. **(NEW)** The method of claim 1 wherein the layer of high temperature oxide is formed by LPCVD process.

22. **(NEW)** The method of claim 7 wherein the layer of high temperature oxide is formed by LPCVD process.

23. **(NEW)** A method of making a flash memory cell including a substrate and a floating gate, the method comprising:

depositing an insulator layer of high quality oxide on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls of high quality oxide around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

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